ADVANCE INFORMATION

7114
4-MEGABIT BUBBLE MEMORY

OPERATING FREQUENCY		CASE OPERATING TEMP. (°C)	NON-VOLATILE STORAGE (°C)
100 KHz	50 KHz		
7114 A-1	7114-1	0→75	−40→+90
7114 A-4	7114-4	10→55	−20→+75

- **4,194,304 Bits of Usable Data Storage**
- **Non-Volatile, Solid-State Memory**
- **True Binary Organization: 512-Bit Page and 8,192 Pages**
- **Major Track–Minor Loop Architecture**
- **Redundant Loops with On-Chip Loop Map and Index**
- **Block Replicate for Read; Block Swap for Write**
- **Single-Chip 20-Pin Dual In-Line Package**
- **Small Physical Volume**
- **Maximum Data Rate 400 Kbit/Sec (7114A)**
- **Average Access Time 40 msec (7114A)**

The Intel Magnetics 7114 (unless otherwise indicated 7114 refers also to 7114A) is a very high-density 4-megabit non-volatile, solid-state memory utilizing magnetic bubble technology. The usable data storage capacity is 4,194,304 bits. The defect-tolerant design incorporates redundant storage loops. The gross capacity of Intel Magnetics bubble memory is 5,242,880 bits.

The 7114 has a true binary organization to simplify system design, interfacing, and system software. The device is organized as 512 data storage loops each having 8,192 storage bits. When used with Intel Magnetics complete family of support electronics, the resultant minimum system is configured as 512K bytes of usable data storage. The support circuits also provide automatic error correction and transparent handling of redundant loops.

The 7114 has a major track–minor loop architecture. It has separate read and write tracks. Logically, the data is organized as a 512-bit page with a total of 8,192 pages. The redundant loop information is stored on-chip in the boot loop along with an index address code. The 7114 provides totally non-volatile data storage when operated within the stated limits.

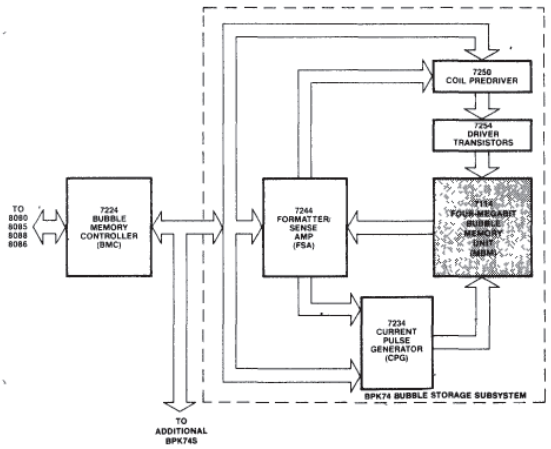


Figure 1. Block Diagram of Single Bubble Memory System—512K Bytes

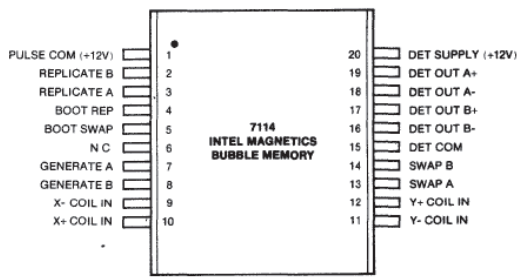


Figure 2. Pin Configuration

NOVEMBER 1982
ORDER NUMBER: 210763-001

Table 1. 7114 Pin Description

Symbol	Pin#	Name and Function
BOOT.REP	4	Two-level current pulse input for reading the boot loop.
BOOT.SWAP	5	Single-level current pulse for writing data into the boot loop. This pin is normally used only in the manufacture of the MBM.
DET.COM	15	Ground return for the detector bridge.
DET.OUT	16–19	Differential pair (A+, A− and B+, B−) outputs which have signals of several millivolts peak amplitude.
DET.SUPPLY	20	+12 volt supply pin.
GEN.A and GEN.B	7, 8	Two-level current pulses for writing data onto the input track.
PULSE.COM	1	+12 volt supply pin.
REP.A and REP.B	3, 2	Two-level current pulses for replicating data from storage loops to output track.
SWAP.A and SWAP.B	13, 14	Single-level current pulse for swapping data from input track to storage loops.
X−.COIL.IN, X+.COIL.IN	9, 10	Terminals for the X or inner coil.
Y−.COIL.IN, Y+.COIL.IN	11, 12	Terminals for the Y or outer coil.

The 7114 is packaged in a dual in-line leaded package complete with permanent magnets and coils for the in-plane rotating field. In addition, the 7114 has a magnetic shield surrounding the bubble memory chip to protect the data from external magnetic fields.

The operating data rate is 400 Kbit/sec for 7114A, and 200 Kbit/sec for 7114. The 7114 can be operated asynchronously and has start/stop capability.

GENERAL FUNCTION DESCRIPTION

The Intel Magnetics 7114 is a 4-megabit bubble memory module organized as two identical 2,048K binary half sections. See Major Track–Minor Loop architecture diagram. Each half section is in turn organized as four 512K subsections referred to as octants.

The module consists of a bubble die mounted in a substrate that accommodates two orthogonal drive coils that surround the die. The drive coils produce a rotating magnetic field in the plane of the die when they are excited by 90° phase-shifted triangular current waveforms. The rotating in-plane field is responsible for bubble propagation. One drive field rotation propagates all bubbles in the device one storage location (or cycle). The die-substrate-coil subassembly is enclosed in a package consisting of permanent magnets and a shield. The shield serves as a flux return path for the permanent magnets in addition to isolating the device from stray magnetic fields. The permanent magnets produce a bias field that is nearly perpendicular to the plane of the die. This field supports the existence of the bubble domains.

The package is constructed to maintain 1.5 degree tilt between the plane of the bias magnet faces and the plane of the die. This serves to introduce a small component of the bias field into the plane of the die. During operation when the drive coils are energized this small in-plane component is negligible. During standby or when power is removed the small in-plane field ensures that the bubbles will be confined to their appropriate storage locations. The direction of the in-plane field introduced by the package tilt (holding field) is coincident with the 0° phase direction of the drive field.

Architecture

A 7114 octant subsection is composed of the following elements shown on the architecture diagram.

STORAGE LOOPS

Each octant subsection contains eighty identical 8,192-bit storage loops to provide a total maximum capacity of 655,360 bits. The excess storage is provided for two purposes: a) it allows a redundancy scheme to increase device yield; and b) it provides the extra storage required to implement error correction.

REPLICATING GENERATOR (GEN)

The generator operates by replicating a seed bubble that is always present at the generator site (GEN).

INPUT TRACK AND SWAP GATE

Bubbles following generation are propagated down an input track. Bubbles are transferred to/from the input track from/to the 80 storage loops via series-connected swap gates spaced every two propagation cycles along the track. The swap gate's ability to transfer bubbles in both directions during an operation eliminates the overhead associated with removing old data from the loops before new data can be written. The swap gate is designed to function such that the logical storage loop position occupied by the bubble transferred out of each loop is filled by the bubble being transferred into each loop. Transferred-out bubbles propagate down the remaining portion of the input track where they are dumped into a bubble bucket guard rail.

OUTPUT TRACK AND REPLICATE GATE

Bubbles are read out of the storage loops in a non-destructive fashion via a set of replicate gates. The bubble is split in two. The leading bubble is retained in the storage loop and the trailing bubble is transferred onto the output track. Replicate gates are spaced every two propagation cycles along the output track.

DETECTOR

Bubbles, following replication, are propagated along the output track to a detector that operates on the magneto-resistance principle. The cylindrical bubble domains are stretched into long strip domains by a chevron expander and are then propagated to the active portion of the detector. The detector consists of a thin film, lying underneath a stack of chevrons, through which a current is passed. As the strip domain propagates below the thin-film detector, its magnetic flux causes a fractional change in film resistance which produces an output signal of several millivolts. The strip domain following detection is propagated to a bubble bucket guard rail. A "dummy" detector stack sits in the immediate vicinity. It is connected in series with the active detector and serves to cancel common mode pickup which originates predominately from the in-plane drive field.

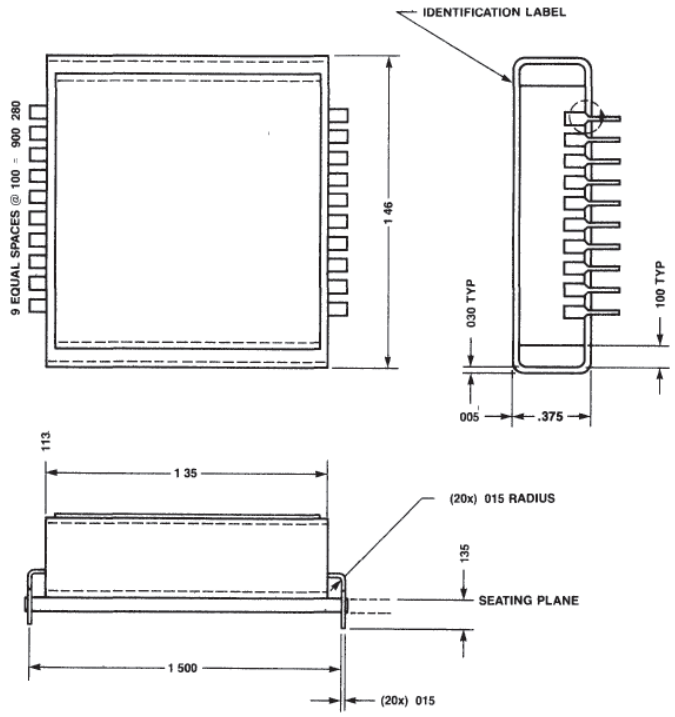
BOOT LOOP, BOOT SWAP, AND BOOT REPLICATE

One of the four octants in each half chip contains a functionally active Boot Storage Loop. This loop is used to store:

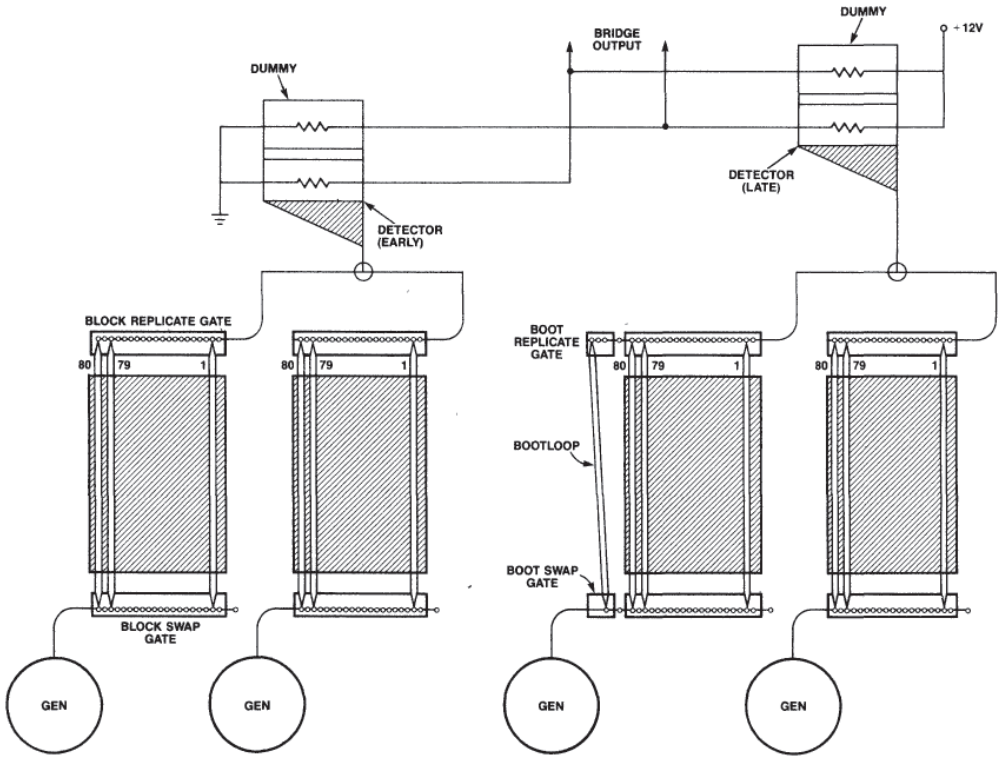
a) A loop mask code that defines which loops within the main storage area should be accessed. Faulty loops are "masked out" by the support electronics.

b) A synchronization code that assigns data addresses (pages) to the data in the storage loops. Since bubbles move from one storage location to the next every field rotation, the actual physical location of a page of data is determined by the number of field rotations that have elapsed with respect to a reference.

The boot loop is read from and written into via the same input and output tracks as the main storage loops. However, it has independently accessed swap and replicate gates. The boot swap, under normal circumstances, is intended only to be used during basic initialization at the factory at which time loop mask and synchronization codes are written. The boot replicate is intended to be accessed every time power is applied to the bubble module and its peripheral control electronics. At such a time, the control electronics would read and store the mask information, plus utilize the synchronization information to establish the location of the data circulating within the loops.



PACKAGE OUTLINE



MAJOR TRACK–MINOR LOOP ARCHITECTURE OF 7114 (ONE HALF SHOWN).

Figure 3. Package Outline and Device Architecture

ABSOLUTE MAXIMUM RATINGS*

Operating Case Temperature ..... 0°C to 75°C Case
Relative Humidity 95%
Shelf Storage Temperature (Data Integrity Not Guaranteed) ..... −65°C to +150°C
Voltage Applied to DET.SUPPLY ..... 14 Volts
Voltage Applied to PULSE.COM ..... 12.6 Volts
Continuous Current between DET.COM and Detector Outputs ..... 10 mA
Coil Current ..... 2.5A D.C. or A.C. RMS
External Magnetic Field for Non-Volatile Storage ..... 20 Oersteds
Non-Operating Handling Shock 200G
Operating Vibration (2 Hz to 2 KHz) 20G

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS (T_C = Range Specified on First Page)

Parameter	Limits			Unit
	Min.	Nom.[1]	Max.	
RESISTANCE: PULSE.COM to GEN.A or GEN.B	12	30	58	ohms
RESISTANCE: PULSE.COM to REP.A or REP.B	13	27	35	ohms
RESISTANCE: PULSE.COM to SWAP.A or SWAP.B	20	47	71	ohms
RESISTANCE: PULSE.COM to BOOT.REP	3.5	8	23	ohms
RESISTANCE: PULSE.COM to BOOT.SWAP	5	20	49	ohms
RESISTANCE: DET.OUT A+ to DET.OUT A−	770	1190	2200	ohms
RESISTANCE: DET.OUT B+ to DET.OUT B−	770	1190	2200	ohms
RESISTANCE: DET.COM to DET.SUPPLY	560	950	2100	ohms

NOTE:
1 Nominal values are measured at 25°C.

DRIVE REQUIREMENTS (T_C = Range specified on First Page) (See note 2) Vdd = 12V ±5%

Symbol	Parameter	7114			7114A			Units
		Min.	Nom.[1]	Max.	Min.	Nom.[1]	Max.	
f_R	Field Rotation Frequency	49.95	50.00	50.05	99.90	100.00	100.10	KHz
I_{px}	X.Coil Peak Current		.58			1.6		A
I_{py}	Y.Coil Peak Current		.74			2.1		A
Θ_{1x}	X.Coil Positive Turn-On Phase	268	270	272	268	270	272	Degrees
Θ_{2x}	X.Coil Positive Turn-Off Phase	16	18	20	16	18	20	Degrees
Θ_{3x}	X.Coil Negative Turn-On Phase	88	90	92	88	90	92	Degrees
Θ_{4x}	X.Coil Negative Turn-Off Phase	196	198	200	196	198	200	Degrees
Θ_{1y}	Y.Coil Positive Turn-On Phase	0	0	0	0	0	0	Degrees
Θ_{2y}	Y.Coil Positive Turn-Off Phase	106	108	110	106	108	110	Degrees
Θ_{3y}	Y.Coil Negative Turn-On Phase	178	180	182	178	180	182	Degrees
Θ_{4y}	Y.Coil Negative Turn-Off Phase	286	288	290	286	288	290	Degrees
P_T	Total Coil Power		1.5			2.9		Watts
R_x	X.Coil D.C. Resistance		7.4			1.0		Ohms
R_y	Y.Coil D.C. Resistance		3.3			0.4		Ohms
L_x	X.Coil Inductance		89			15		μH
L_y	Y.Coil Inductance		78			14		μH

NOTES:
1. Nominal values are measured at T_C = 25°C.
2. See Figure 4 for test set-up and X-Y Coil waveform.

CONTROL PULSE REQUIREMENTS (see Notes 2 and 3) (T_C = Range Specified on First Page)

Pulse	Current (mA)			Phase of Leading Edge (Degrees)			Width (Degrees)		
	Min.	Nom.	Max.	Min.	Nom.[1]	Max.	Min.	Nom.[1]	Max.
GEN.A, GEN.B CUT	39	44	50	275 95	279 (late) 99 (early)	283 103	6	9	13.5
GEN.A, GEN.B TRANSFER	25	29	33	275 95	279 (late) 99 (early)	283 103	86	90	94
REP.A, REP.B CUT	130	148	165	284	288	292	6	9	13.5
REP.A, REP.B TRANSFER	100	115	130	284	288	292	86	90	94
SWAP	140	152	165	176	180	184	513	517	521
BOOT.REP CUT	33	38	42	284	288	292	6	9	13.5
BOOT.REP TRANSFER	25	29	33	284	288	292	86	90	94
BOOT SWAP	35	39	44	176	180	184	See Note 4		

NOTES:
1. Nominal values are at T_C = 25°C.
2. Pulse timing is given in terms of the phase relations as shown below. For example, a 7114 operating at t_R = 50.000 KHz would have a REP.A transfer width of 90° which is 5 μsec.
3. Two level pulses are described as shown below in Figure 5.
4. BOOT.SWAP is not normally accessed during operation. It is utilized at the factory to write the index address and redundant loop information into the bootstrap loops before shipment.

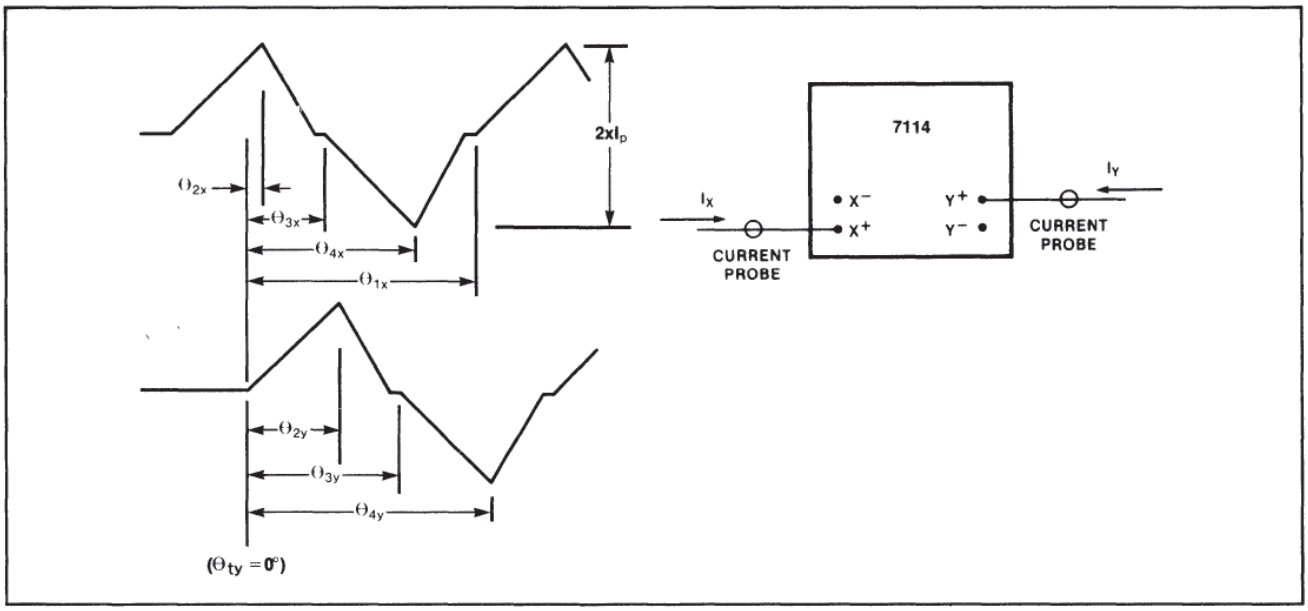


Figure 4. X-Y Coil Waveforms and Test Set-Up

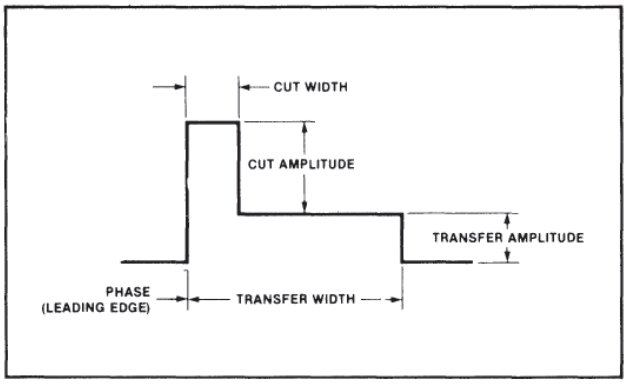


Figure 5. Two-Level Current Pulse

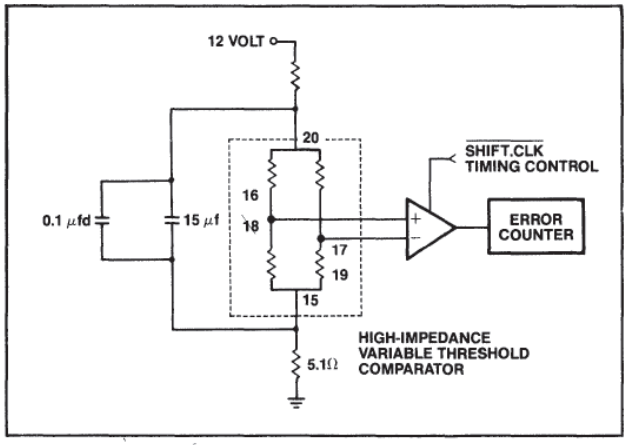


Figure 6. Test Set-Up for Output Voltage Measurement

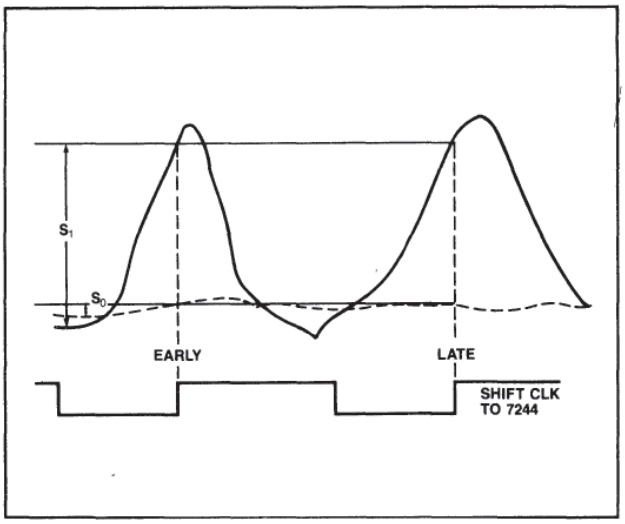


Figure 7. Detector Output Waveforms

OUTPUT CHARACTERISTICS (T_C = Range Specified on Front Page)

Symbol	Nom.	Units	Test Conditions
S_1	18	mV	See notes
S_0	1	mV	1, 2

NOTES:
1 Nominal values are measured at T_C = 25°C
2 See Figure 6 for test set-up, and Figure 7 for detector output waveforms and timing